REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	31 MAY 92	Annual Technical 1 JUN 91 - 31 MAY 92

4. TITLE AND SUBTITLE
Large Signal Characterization and Modeling of Heterojunction Bipolar Transistors

5. FUNDING NUMBERS
G AFOSR-90-0302
PR 2305/R1

(2)

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8. PERFORMING ORGANIZATION REPORT NUMBER
AFOSR-TR- 92 0662

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AFOSR/NE
Building 401
Bolling AFB DC 20332-6448

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
2305/R1

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

The high power operation of the heterojunction bipolar transistor (HBT) has been analyzed by experimentally determining the junction temperature and separating temperature effects from other high power effects. In addition, an HBT large signal model has been developed that is valid for the linear, saturation, and cutoff regions, with temperature effects included. This model has been implemented in a commercial harmonic balance simulator LIBRA from EEsof. making it particularly suitable for the design and simulation of HBT microwave power integrated circuits.

14. SUBJECT TERMS
Heterojunction Bipolar Transistor
Large Signal Modeling: Thermal Effects

15. NUMBER OF PAGES
12

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	SAR

Contents

Figures

1. Objectives

The main objective of this three year research effort is to investigate the large-signal characteristics of a heterojunction bipolar transistor (HBT) and to apply the knowledge gained to improve both the HBT device and circuit design.

Through innovative approaches for large-signal characterization and modelling, the following will be achieved:

- o Effective parameter extraction from DC and RF measurements to provide feedback to HBT device design.
- o Accurate large-signal measurement in the frequency domain, taking into account the effects of harmonic magnitudes and phases.
- o Non-linear equivalent circuit model for efficient de-embedding from DC and RF characteristics.

2. Progress

During this second year of the research effort, many types of measurements have been set up and performed to fully characterize the heterojunction bipolar transistor (HBT). The measurements include DC, pulsed, RF, small signal, power, harmonic and elevated temperature tests as will be described in the following. Most measurements were performed on-wafer which eliminates substrate thinning, dicing and packaging and allows for rapid characterization. The devices characterized were GaAs/AlGaAs HBTs fabricated by the Air Force Wright Laboratory with either three 1μ x 8μ emitters, or a single 1μ x 8μ emitter. The Al concentration at the base emitter junction was graded from 0.3 to 0.0. The substrate thickness was 625μm.

The high power operation of the HBT has been analyzed by experimentally determining the junction temperature and separating temperature effects from other high power effects.

In addition, an HBT large signal model has been developed that is valid for the linear, saturation , and cutoff regions, with temperature effects included. This model has been implemented in a commercial harmonic balance simulator LIBRA from EEsof, making it particularly suitable for the design and simulation of HBT microwave power integrated circuits.

2.1 DC and RF Characterization

The equipment used for DC characterization and device biasing includes an HP4142 Semiconductor Parametric Analyzer equipped with three source and monitoring units of either voltages or currents. For high frequency measurements the equipment used included an HP8510-B, a 40 GHz network analyzer with a two port S-parameter test-set, and a HP70206A 26 GHz spectrum analyzer. Calibration of the test equipment was performed on-wafer using a Tektronix calibration substrate.

The DC characterization performed on the HBTs included common emitter I-V, collector and base current vs base voltage, floating collector, and breakdown measurements. All of these

result in parameters used as starting points for determining RF equivalent circuit parameters.

RF small-signal S-parameter measurements were performed at bias points over the entire active region of the HBTs. These sets of data were used to extract model element values using optimization techniques. The bias-dependent element values where then used in the large signal model. Power and harmonic measurements were performed up to 2 W/mm and used to confirm large signal model predictions.

2.2 Elevated Temperature Measurements

For on-wafer measurements even at moderate power levels, un-packaged and un-thinned HBTs exhibit significant thermal effects. For the HBT, the undesirable thermal effects result in a reduction of gain and an significant change in base-emitter diode characteristics.

To analyze the thermal effects, DC measurements were performed on an HBT inside an oven. Full sets of I-V characteristics were measured from 23°C to 200°C. The base-emitter voltage (V_{bc}) was monitored as a function of temperature and collector voltage for different base currents. V_{be} was found to be a very accurate indication of the actual junction temperature and is shown in Figure 1 to be linear to within 0.4%. For this set of data the collector voltage was chosen to be in the forward active region, but kept at a minimum to limit the power dissipation. V_{be} was, however, found to be independent of collector voltage at low power densities where self heating is negligible.

For room temperature I-V measurements the base-emitter voltage is monitored and used to calculate the junction temperature. For this device, having a 625 μm substrate, all points in the forward active region are consistent with a thermal resistance of 2.9 C/mW to within 10% as seen in Figure 2. This thermal resistance is from the base-emitter junction to the ambient, and is used to obtain the temperature contours on a plot of I-V characteristics as seen in Figure 3.

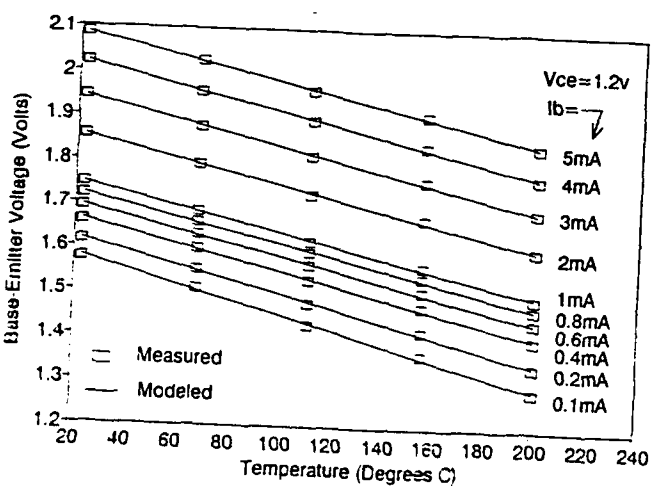

Figure 1. The dependence of base-emitter voltage on ambient temperature.

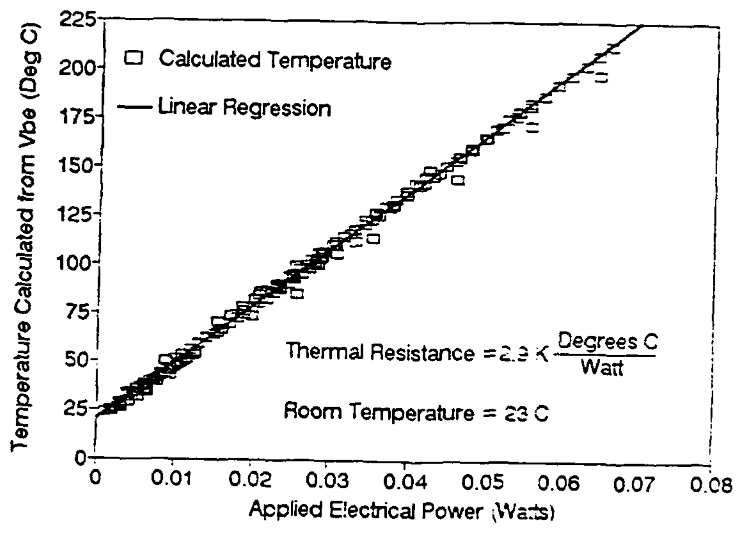

Figure 2. Junction Temperature Calculated from the base-emitter voltage.

The gain degradation as the junction temperature increases is shown in Figure 4. The degradation is essentially linear at -0.0038 /C. The data in this figure includes the forward active region up to where the collector current increases through breakdown. Extrapolating these lines back to room temperature, the Kirk effect can be seen to reduce gain at high base currents (I_b) independent of the temperature effect. Notice that the maximum gain occurs at I_b = 4 mA, and the Kirk effect causes a reduction of gain at I_b = 5 mA.

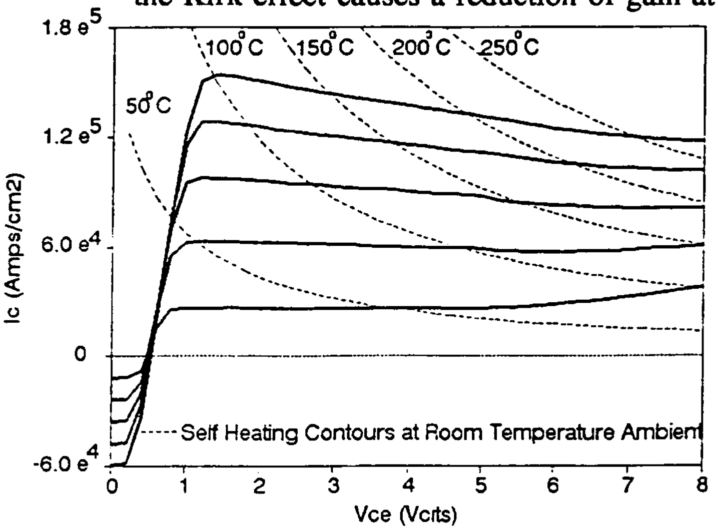

Figure 3. HBT self-heating temperature contours.

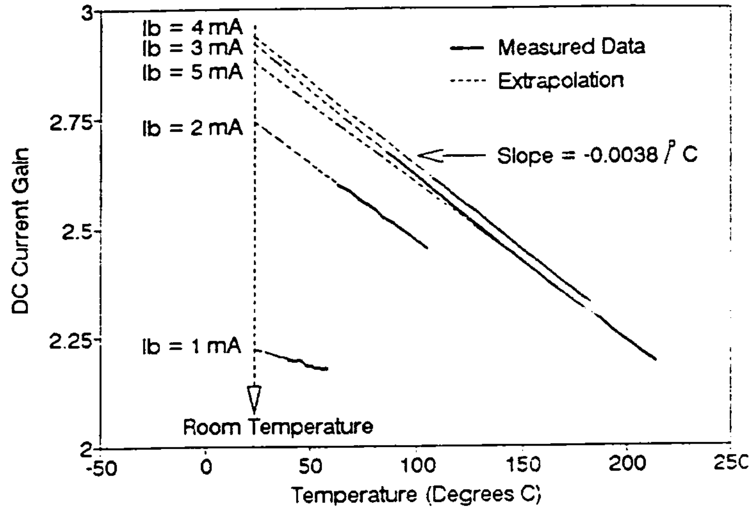

Figure 4. Gain degradation with increasing junction temperature.

2.3 Pulsed Measurements

Pulsed DC testing was also used to quantify the effects of high junction temperatures on the HBT. Pulse testing has been used to measure the I-V characteristics before the base-emitter junction temperature rises through self-heating. Base voltage pulses of 1 μs were applied at a repetition rate of 1 ms and duty cycle of 0.1%.

Figure 5 shows the circuit used to apply and measure the pulsed IV characteristics. R_1 and R_2 are used as a voltage divider in order to use the full voltage range of the source for the base emitter voltage. The series combination is also designed to match the pulse generator near 50Ω. R_b is used to measure Ib using an oscilloscope while the small capacitor C_b stabilizes ringing on the rise and fall of the base pulse. On the collector side, R_c is used to measure the collector current and C_c maintains a constant DC voltage reference.

All pulsed measurements were performed manually using an oscilloscope to ensure accuracy and base-collector current correspondence with time. The base and collector current were measured at 110 ns after the pulse edge, to avoid any rise-time effects. Figure 6 shows the significant reduction in negative differential resistance when using pulsed measurements, reflecting the device's true characteristics in the absence of self heating.

As mentioned earlier, maximum gain values in the absence of self heating can be extrapolated from the thermal measurement data of Figure 4. The pulsed measurements confirm these predicted gain values which are also indicated in Figure 6. For longer pulse widths, the amount of time required to heat the junction can be observed with this pulsed technique, where

an approximate thermal time constant of 0.5 μs has been measured.

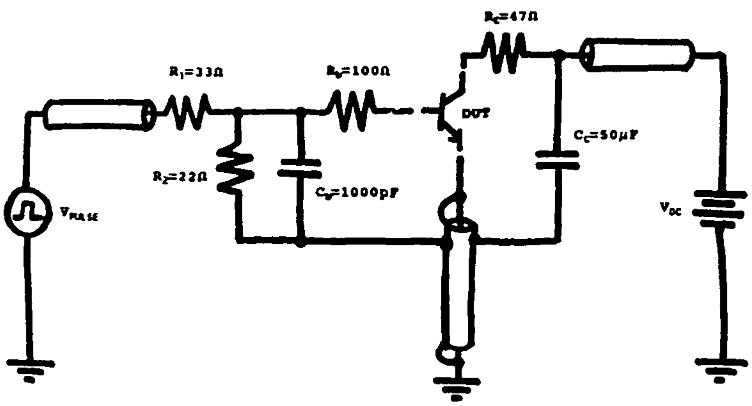

Figure 5. Pulsed measurement setup.

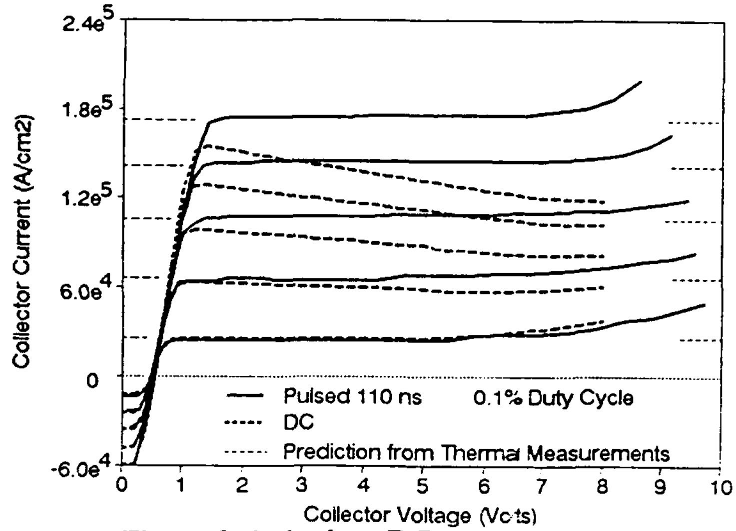

Figure 6. Pulsed vs. DC measurements.

2.4 Power and Harmonic Large Signal Transport Modeling

Figure 7 shows our HBT large signal equivalent circuit based on the Ebers-Moll model with some modifications. Seven elements are nonlinear, the base-emitter and base-collector extrinsic conductance and capacitance, and the effective current gain, β_{eff}. All nonlinear formulas are in terms of exponentials because of their efficient computation and continuous high-order derivatives.

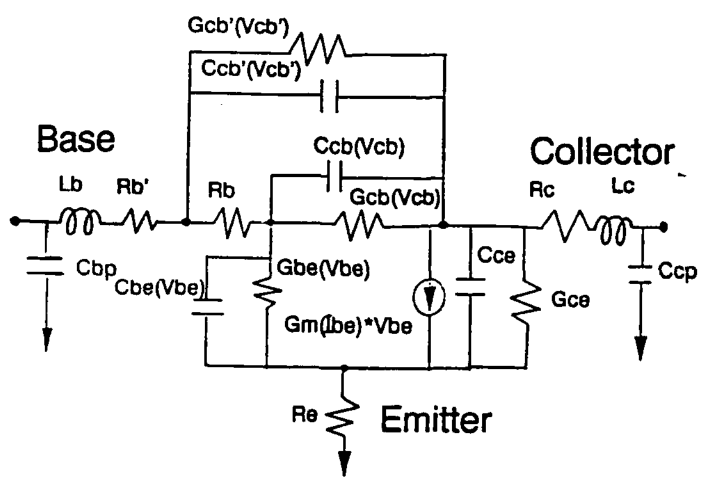

Figure 7. Equivalent circuit model for a power HBT.

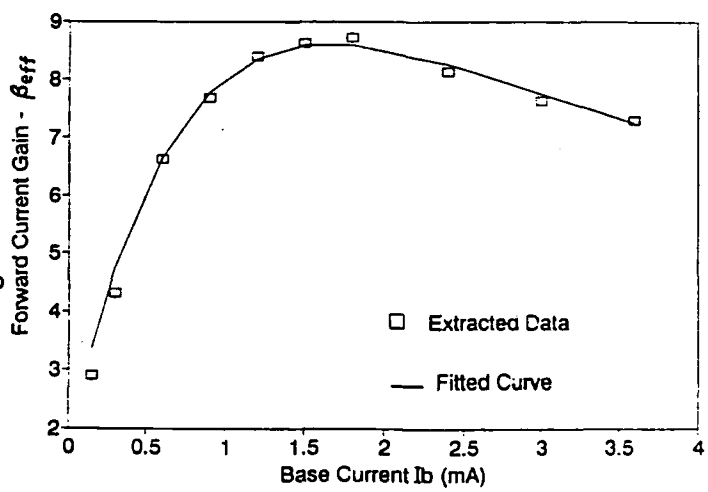

Figure 8. Fitted vs. measured current gain.

To minimize low-frequency effects due to surface traps, etc., the equivalent circuit elements were extracted solely from small-signal S-parameters over a wide bias range. An analytic procedure for direct extraction of the HBT's parasitic and intrinsic element values was

developed. The current gain, transit times and parasitic emitter and base resistance were extracted from low frequency S-parameters by a simplified equivalent circuit. The parasitic collector resistance and inductance was extracted from S-parameters at the zero collector current offset points at high base currents. The base-collector parameters were extracted from reverse-bias data. Knowing the parasitic parameter values the intrinsic parameter values were evaluated according to the equivalent circuit. Successive steps are used to fit the nonlinear function to the bias-dependent element values. Figure 8 illustrates the fitting of β_{eff} where two exponential terms are used in order to simulate the gain reduction both at high and low base currents.

This equivalent circuit model has been implemented in LIBRA, a harmonic balance simulator from EEsof Inc., and verified with 50 Ω on-wafer power measurements. The 5.5 GHz input was pulsed for 5 s at 40 KHz in order to avoid overheating due to high power dissipations. The HBT was biased in Class A with a constant base-emitter voltage which yielded a maximum RF output power level of 2 W/mm. Careful calibration was performed to account for all losses in the cables, probes and analyzer. Figure 9 shows the excellent agreement between measured and modeled output power characteristics. The fundamental output power saturates due to the output swinging from the saturation to the cutoff regions as verified by waveform simulations.

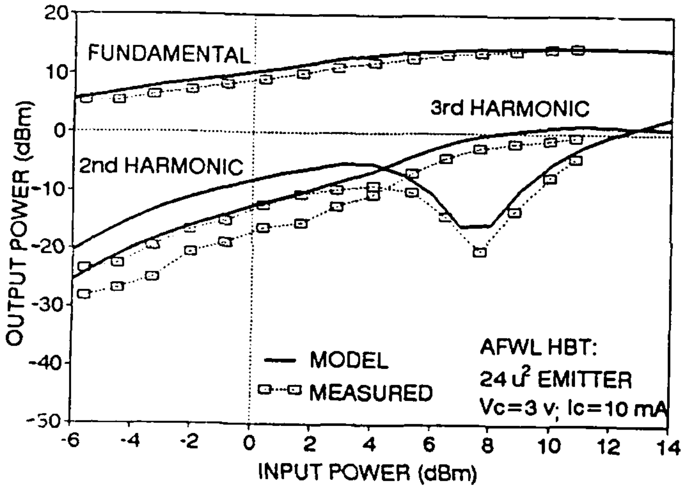

Figure 9. Simulated output power vs. input power.

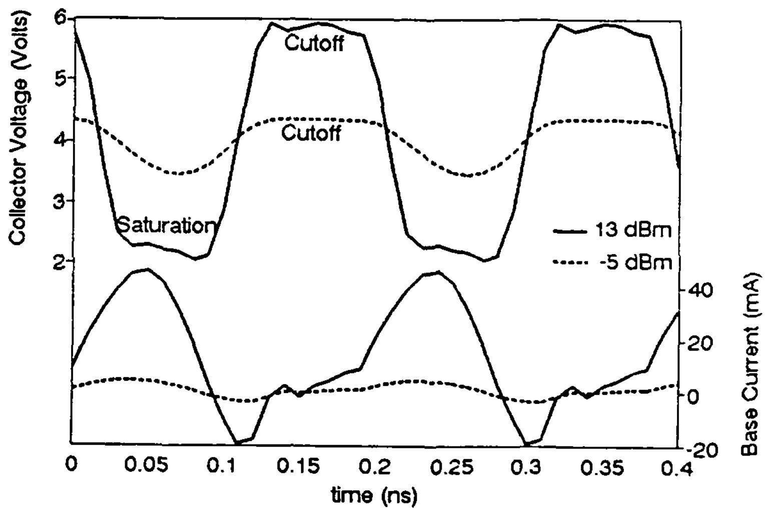

Figure 10. Simulated waveforms of nodal currents and voltages.

Figure 10 shows the waveforms for collector voltage and base current at an input power of 5 and 13 dBm. The collector voltage is clipped at both the top and bottom when the HBT swings into saturation and cutoff. In addition to causing power saturation, this also causes the second and fourth harmonics to approach a minimum while the third harmonic approaches a maximum. The waveforms also show that the base current swings negative before it settles to a small cutoff value indicating a relatively large amount of stored charge that must be depleted before the base-emitter voltage becomes negative. Likewise we have found a relatively large base-emitter transit time for this HBT of 5 ps.

2.5 Large Signal Thermal Modeling

In this same transport model, the thermal effects described earlier are also included. These effects include the linear decrease in V_{be} with temperature as seen n Figure 1, and the linear gain degradation with temperature as seen in Figure 4. In the model, the transient temperature of the device is calculated based on the total power dissipated, the thermal resistance, and the thermal time constant. Results of the large signal model have been compared to pulsed and DC measurements as seen in Figures 11, 12, and 13. An additional useful product of this model is the determination of the actual junction temperature as seen n Figure 14 for a pulsed simulation.

Because of the long time constant, the microwave CW operation simply causes a constant junction temperature with time, and the model adjusts the I-V relationships accordingly. The model s useful for simulating device characteristics with different heat-sink configurations, allowing the use of on-wafer measurements to predict packaged device performance. The model also gives an indication of the thermal limitations of the device in all modes of operation including DC, pulsed and RF.

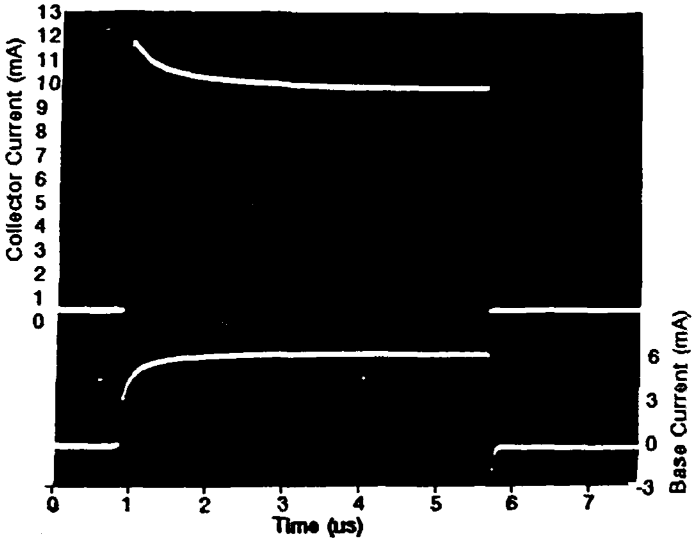

Figure 11. Measured response of I_b and I_c to a 5 μs base voltage pulse.

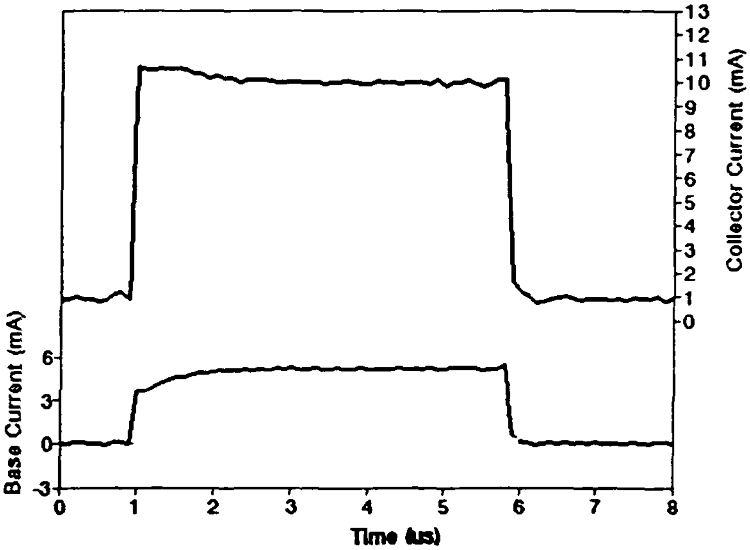

Figure 12. Simulated response of I_b and I_c to a 5 μs base voltage pulse.

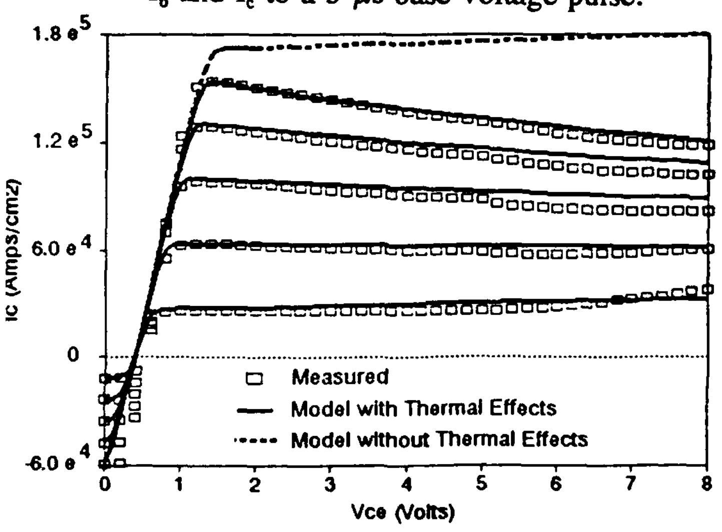

Figure 13. Simulated and measured HBT collector characteristics.

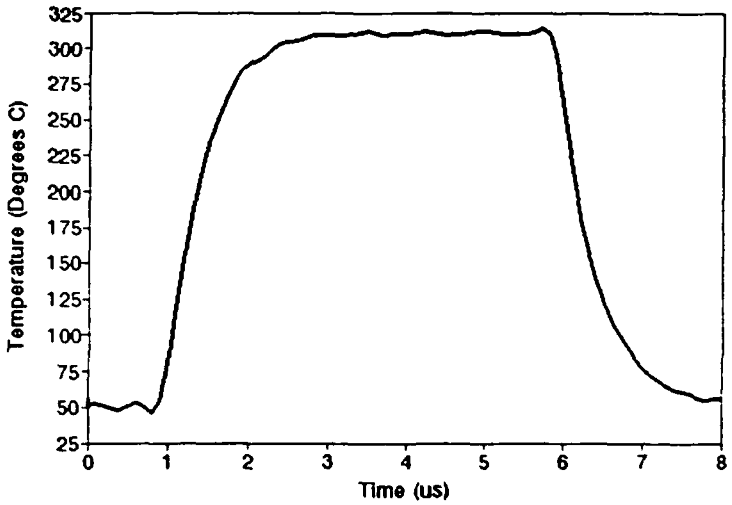

Figure 14. Modeled junction temperature during the simulation of Figure 13.

2.6 Conclusion

Extensive DC and RF characterization has been performed for evaluation of device performance and extraction of bias-dependent model elements for use in a large signal model. Pulse testing and elevated temperature measurements have been performed, showing how thermal effects can be quantified and isolated from other gain-degrading effects. This leads to an accurate understanding of the HBT at high power densities hence accurate modeling of the many interdependent effects.

Also for use in high power applications, a true large signal nonlinear model has been developed which incorporates the effects of saturation, cutoff, the Kirk effect, and the thermal effects. The model has been implemented in a harmonic balance simulator with excellent agreement to on-wafer power and harmonic measurements as well as DC and pulsed measurements. The model also gives access to RF current an voltage waveforms as well as low frequency temperature waveforms which were beyond the capabilities of laboratory experiments. By knowing such information, many mechanisms can be understood such as the cause of output saturation and the behavior of harmonics.

2.7 Future Work

Work will continue along two main paths. One path will be to perform an in-depth study of the HBT physics and obtain a concise physical model applicable to DC through RF operation. This will be used to modify the existing large signal model which is mostly based on empirical formulas where parameter values are derived through curve-fitting to measured data. A more physically meaningful model will increase its ability to predict the performance of new device designs.

Another path will be the continued investigation of the thermal effects on the large signal behavior of the HBT. Elevated temperature S-parameter measurements will be performed on several devices at many bias-points. Model element values will be extracted as before, and analyzed specifically for their dependence on temperature. These effects will be added to the existing model and confirmed against actual large signal power and harmonic measurements.

By using our newly acquired HP70820A Microwave Transition Analyzer we will be measuring both the magnitude and phase of the output harmonics. This allows the Analyzer to reconstruct the actual waveform of the output signal with harmonics up to 40 GHz providing valuable waveform information. This Analyzer will also allow us to measure pulsed power responses which will be used to analyze the high and low frequency thermal effects together.

2.8 Acknowledgements

The authors wish to thank the Ar Force Wright Laboratory, particularly G.J. Trombley, M.E. Cheney, and C.I. Huang, for supplying devices and helpful discussions.

3. Publications

D.S. Whitefield, C.J. Wei, J.C.M. Hwang, "High Power Characterization and Modeling of Heterojunction Bipolar Transistors," 1992 IEEE Princeton Section Sarnoff Symposium Digest, Session II.

Manuscripts in preparation planned for later submission:

D.S. Whitefield, C.J. Wei, J.C.M. Hwang, "Temperature Dependent Large Signal Model of Heterojunction Bipolar Transistors," 1992 GaAs IC Symposium.

4. Professional Personnel

Dr. J.C.M. Hwang
Professor of Electrical Engineering and
Director of Compound Semiconductor Technology Laboratory, Lehigh University.

Dr. C.J. Wei
Research Scientist, Compound Semiconductor Technology Laboratory, Lehigh University.

D.S. Whitefield
Graduate Student and Research Assistant.
M.S., Electrical Engineering, Lehigh University, 1991. Thesis: Large Signal Characterization and Modeling of Heterojunction Bipolar Transistors.

5. Presentations

- Location: Wright Laboratory, Wright Patterson AFB, Ohio. December, 1991.
  Speaker: D.S. Whitefield
  Title: HBT Thermal Effects.

- Location: Wright Laboratory, Wright Patterson AFB, Ohio. December 1991.
  Speaker: C.J. We
  Title: Large Signal Modeling of the Heterojunction Bipolar Transistor.

- Location: David Sarnoff Research Center, Princeton NJ. March, 1992.
  Speaker: D.S. Whitefield
  Title: High Power Characterization and Modeling of Heterojunction Bipolar Transistors.

- Location: Wright Laboratory, Wright Patterson AFB, Ohio. April, 1992.
  Speaker: J.C.M. Hwang
  Title: High Power Characterization and Modeling of Heterojunction Bipolar Transistors.

6. Interactions

Dr. Hwang is a consultant to the Air Force Wright Laboratory in the areas of MMIC processing and material/device correlation. Dr. Hwang spends 20% of his time at Wright Laboratory and both written and oral progress reports on HBTs are provided regularly to Dr. Chern Huang and his colleagues. The HBT devices used for this work were fabricated at Wright Laboratory using their in-house MBE process.

D.S. Whitefield s a Second Lieutenant in the Air Force Reserves, currently on a four year educational delay to complete his Ph.D. degree n Electrical Engineering. In December 1991, D.S. Whitefield spent one week at the Ar Force Wright Laboratory discussing microwave device fabrication, characterization, and modeling.

Dr. Wei also spent one week in December 1991 at the Air Force Wright Laboratory discussing microwave device fabrication, characterization, and modeling.

7. Inventions

There have been no inventions for this report period (DD Form 882 Attached).